Abstract

The invention relates to a method for the planarization of a semiconductor structure comprising a substrate, in which several sub-structures (STI; AA; AA'; AA";) are provided. said sub-structures (STI; AA; AA'; AA") having a first sub-structure (AA') with planar regions (PS) and first trench regions (DT). A layer to be planarized is applied over the semiconductor structure, said layer having appropriate recesses above the first trench regions (DT) of the first sub-structure (AA'). The method comprises the following steps: pre-planarization of the layer to be planarized by an etching step, using a pre-planarization mask, then subsequent planarization of the layer to be planarized by a chemical-mechanical polishing step. According to the invention, a first region (B1) is formed on the layer to be planarized above the first sub-structure (AA') by means of the pre-planarization mask, said region having a predetermined grid of masked and unmasked sections (M1; O1) are arranged in such a way that they respectively cover both first trench regions (DT) and planar regions (PS), and a supporting structure for the chemical-mechanical polishing step, which corresponds with the masked sections (M1) of the grid, is created by the etching step, using the pre-planarization mask.